IN THE CLAIMS:

Please amend claims 1-4, 6, 11 and 15 as follows:

1. (Currently Amended) A storage device control unit for performing data writing/reading to/from a storage device responding to a request coming from an information processor via a network, the unit comprising:

a communications interface section for carrying out communications with the information processor;

a storage device interface section for carrying out communications with the storage device;

a cache memory section including first cache memory for storage of data coming and going between the information processor and the storage device; and

[[a]] an internal connection section for connecting all together the communications interface section, the storage device interface section, and the cache memory section for communications thereamong, wherein

the internal connection section is provided with second cache memory for storage of data same as the [[one]] data stored in the first cache memory.

2. (Currently Amended) The storage device control unit according to claim 1, wherein the communications interface section and the storage device interface section each include an access control section for transmitting, to the connection section, first access/no access information for indicating whether or not to make access to the second cache memory together with an access request to the first cache memory, and

the connection section includes a control section for controlling whether or not to make access to the second cache memory based on the first access/no access information included in the access request received from the access control section.

3. (Currently Amended) The storage device control unit according to claim 1, wherein the cache memory section includes:

a memory control section for controlling writing/reading of the data to/from the first cache memory; and

third memory being accessible by the memory control section, and storing data same as the one stored in the first cache memory.

4. (Currently Amended) The storage device control unit according to claim 3, wherein

the communications interface section and the storage device interface section each include an access control section for transmitting, to the connection section, second access/no access information for indicating whether or not to make access to the third memory together with an access request to the first cache memory, and

the memory control section controls whether or not to make access to the third memory based on the second access/no access information included in the access request received from the access control section via the connection section.

5. (Original) The storage device control unit according to claim 1, wherein the communications interface section and the storage device interface section each include an access control section for transmitting, to the connection section, addressee information designating as an addressee all of the communications interface sections and all of the storage device interface sections, the communications interface section or the storage device interface section, or the memory section together with the data or control data for controlling transfer of the data, and

the connection section includes a control section for controlling communications with the addressee designated by the addressee

information received from the access control section together with the data or the control data.

6. (Currently Amended) The storage device control unit according to claim 5, wherein the control section of the connection section stores the received data or control data in the second cache memory until a data bus to be used for transferring the data or the control data becomes available.

7. (Original) The storage device control unit according to claim 5, wherein the control section of the connection section transmits, back to an addresser of the received data or control data, information indicating whether or not the received data or control data is transmitted to the addressee within a predetermined time.

8. (Original) The storage device control unit according to claim 5, wherein when the addressee information received together with the data or control data is designating all of the communications interface sections and all of the storage device interface sections as the addressee, the control section of the connection section performs parallel transmission of the received data or control data to the addressee.

9. (Original) The storage device control unit according to claim 1, wherein the communications interface section and the storage device interface section each include an access control section for transmitting, to the connection section, the data or control data for controlling transfer of the data together with priority information with which a priority is set in a transfer process to be executed in the connection section, and

the connection section includes a control section for executing the transfer process based on the priority set in the priority information that is received from the access control section together with the data or the control data.

10. (Original) The storage device control unit according to claim 9, wherein in the priority information, the data or the control data having a first data size

has a higher priority than the data or the control data having a second data size smaller than the first data size.

11. (Currently Amended) The storage device control unit according to claim 1, wherein the first cache memory stores the data coming and going between the information processor and the storage device, and

the control data for controlling the data coming and going.

12. (Original) The storage device control unit according to claim 1, wherein connection among the communications interface section, the storage device interface section, and the connection section, and between the connection section and the cache memory section is established by a data bus that is used for transferring the data coming and going between the information processor and the storage device, and the control data for controlling the data coming and going.

13. (Original) The storage device control unit according to claim 1, wherein the connection section is a high-speed crossbar switch for establishing a network connection among the communications interface section, the storage device interface section, and the cache memory section.

14. (Original) The storage device control unit according to claim 1, wherein the communications interface section, the storage device interface section, the cache memory section, and the connection section are each a unit, and

the storage device control unit includes an attachment section to which the unit is attachable.

15. (Currently Amended) A method for controlling communications between an information processor and a storage device via a network ~~control unit~~ comprising:

providing a storage device control unit including a communications interface section for carrying out communications with an information processor[;], a storage device interface section for carrying out

communications with a storage device[;], a cache memory section including first cache memory ~~for storage of data coming and going between the information processor and the storage device;~~, and [[a]] an internal connection section for connecting all together the communications interface section, the storage device interface section, and the cache memory section for communications thereamong, and the connection section being provided with second cache memory; ~~for storage of~~

storing data coming and going between the information processor and the storage device in the first cache memory; and

storing in the second cache memory data same as the ~~one~~ data stored in the first cache memory~~, wherein~~

~~the communications interface section~~

~~receives a data writing/reading request coming from the information processor to/from the storage device, and~~

~~transmits, to the connection section, an access request to the first memory responding to the request, and~~

~~the connection section~~

~~receives the access request from the communications interface section, and~~

~~controls whether or not to perform operation to the second memory according to details of the access request~~.